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FORM PTO-1390 (Modified) (REV 11-98) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER	U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR)
301/49887	09/581464

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/EP99/07531	October 7, 1999	October 9, 1998

TITLE OF INVENTION

MULTIPLEXER CIRCUIT AND ANALOGUE-TO-DIGITAL CONVERTER

APPLICANT(S) FOR DO/EO/US

Martin SEIFERT, Christoph GOTTSCHALK and Rudiger KOHN

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☐ This is an express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☐ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☒ A copy of the International Search Report (PCT/ISA/210).
8. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.
9. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
10. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
11. ☐ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).

Items 13 to 20 below concern document(s) or information included:

13. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
14. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☒ A **FIRST** preliminary amendment.
16. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
17. ☐ A substitute specification.
18. ☐ A change of power of attorney and/or address letter.
19. ☒ Certificate of Mailing by Express Mail
20. ☒ Other items or information:

Form PCT/RO/101
Cover Page of WO 00/22730
Form PCT/IB/308

U.S. APPLICATION NO (IF KNOWN, SEE 37 CFR)	INTERNATIONAL APPLICATION NO	ATTORNEY'S DOCKET NUMBER
09/581464	PCT/EP99/07531	301/49887

21. The following fees are submitted:.

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :

		CALCULATIONS PTO USE ONLY
☐	Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2) paid to USPTO and International Search Report not prepared by the EPO or JPO	$970.00
☒	International preliminary examination fee (37 CFR 1.482) not paid to USPTO but Internation Search Report prepared by the EPO or JPO	$840.00
☐	International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO	$690.00
☐	International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4)	$670.00
☐	International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4)	$96.00

ENTER APPROPRIATE BASIC FEE AMOUNT =	$840.00	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).	$0.00	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	18 - 20 =	0	x $18.00	$0.00	
Independent claims	1 - 3 =	0	x $78.00	$0.00	
Multiple Dependent Claims **(check if applicable).**			☐	$0.00	
	TOTAL OF ABOVE CALCULATIONS =			$840.00	
Reduction of 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also be filed (Note 37 CFR 1.9, 1.27, 1.28) **(check if applicable).**			☐	$0.00	
	SUBTOTAL =			$840.00	
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (f)).			+	$0.00	
	TOTAL NATIONAL FEE =			$840.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) **(check if applicable).**			☒	$120.00	
	TOTAL FEES ENCLOSED =			$960.00	
				Amount to be: refunded	$
				charged	$

☒ A check in the amount of **$960.00** to cover the above fees is enclosed.

☐ Please charge my Deposit Account No. in the amount of to cover the above fees.
A duplicate copy of this sheet is enclosed.

☒ The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. **04-1105** A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

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SIGNATURE

George W. Neuner
NAME

26,964
REGISTRATION NUMBER

June 7, 2000
DATE

Docket No. 301/49887

IN THE UNITED STATES PATENT OFFICE

APPLICANT: Martin Seifert

Entry of U.S. National Stage of
International application PCT/EP99/07531

For: MULTIPLEXER CIRCUIT AND ANALOGUE-TO-DIGITAL CONVERTER

PRELIMINARY AMENDMENT

Please amend the above application as follows.

IN THE CLAIMS:

Please cancel claims 1-18 and insert new claims 19-36 as follows:

--19. A multiplexer circuit comprising at least two input channels and an output channel, each input channel comprising a first transmission gate which can be switched on by a select signal for connecting the input channel to the output channel, at least one of the input channels comprising a bypass circuit for preventing a current flowing through the first transmission gate from reaching the other input channel, and a second transmission gate, said multiplexer circuit further comprising a control circuit for controlling said bypass circuit.

20. The multiplexer circuit according to claim 19, wherein said control circuit controls said bypass circuit dependent upon a voltage in the input channel.

21. The multiplexer circuit according to claim 19, wherein said control circuit comprises a sense circuit to control said bypass circuit by sensing a voltage in the input channel.

22. The multiplexer circuit according to claim 19 , wherein each input channel comprises a bypass circuit and a second transmission gate.

23. The multiplexer circuit according to claim 22, wherein the bypass circuit is switched on for an input channel which is not selected and is switched off for a selected input channel.

24. The multiplexer circuit according to claim 19, wherein said bypass circuit comprises a pull-down circuit reducing an input voltage for the second transmission gate.

25. The multiplexer circuit according to claim 19, wherein said bypass circuit is controlled by said select signal.

26. The multiplexer circuit according to claim 19, wherein said bypass circuit is an NMOS transistor comprising a gate, a drain and a source, the gate of which is controlled by said select signal, the drain of which is connected with an output of said first transmission gate and the source of which is connected with ground potential.

27. The multiplexer circuit according to claim 19, wherein said bypass circuit comprises a pull-up circuit increasing an input voltage for said second transmission gate.

28. The multiplexer circuit according to claim 27, wherein said pull-up circuit is a PMOS transistor comprising a drain and a source, the drain of which is connected with an output of said first transmission gate and the source of which is connected with a power supply voltage level.

29. The multiplexer circuit according to claim 19, wherein said control circuit controls said bypass circuit by means of said select signal and an input voltage applied to said input channel.

30. The multiplexer circuit according to claim 19, wherein said bypass circuit comprises a pull-down circuit reducing an input voltage for the second transmission gate and a pull-up circuit increasing an input voltage for said second transmission gate, wherein said control circuit controls said pull-up circuit and said pull-down circuit by means of said select signal and an input voltage applied to said input channel.

31. The multiplexer circuit according to claim 30, wherein said bypass circuit comprises (a) an NMOS transistor comprising a gate, a drain and a source, the gate of which is controlled by said select signal, the drain of which is connected with an output of said first transmission gate and the source of which is connected with ground potential and (b) a PMOS transistor comprising a drain and a source, the drain

of which is connected with an output of said first transmission gate and the source of which is connected with a power supply voltage level,

wherein said control circuit comprises a NAND gate the output of which is connected with the gate of said PMOS transistor and a NOR gate the output of which is connected with the gate of said NMOS transistor.

32. The multiplexer circuit according to claim 31, wherein said NAND gate receives the input voltage and the inverter select signal and said NOR gate receives the input voltage and the select signal.

33. The multiplexer circuit according to claim 21, wherein said sense circuit is constructed and adapted to sense a voltage in the input channel at the input of said first transmission gate or between said first transmission gate and said second transmission gate.

34. A multiplexer circuit according to claim 33, wherein a pull-down bypass circuit is formed of a first NMOS transistor having a drain and a source, the drain of which is connected with an output of said first transmission gate and the source of which is connected with the ground level, and

wherein said sense circuit is formed of a PMOS transistor and a second NMOS transistor in series, the second NMOS transistor having a source and a drain, the source of the second NMOS transistor being connected to ground level and the PMOS

transistor having a source and a drain, the source being connected to an output of said first transmission gate, and

wherein the drains of said PMOS transistor and said second NMOS transistor are connected to each other and to the gate of the first NMOS transistor in the bypass circuit.

35. The multiplexer circuit according to claim 33, wherein said pull up bypass circuit is formed of a first PMOS transistor having a drain and a source, the drain of which is connected with an output of said first transmission gate and the source of which is connected with power supply voltage level, and

wherein said sense circuit is formed of a second PMOS transistor and an NMOS transistor in series, the second PMOS transistor and the NMOS transistor each having a source and a drain, the source of the second PMOS transistor being connected to power supply voltage level and the source of the NMOS transistor being connected to an output of said first transmission gate, and

wherein the drains of the second PMOS transistor and the NMOS transistor are connected to each other and to the gate of the first PMOS transistor in the bypass circuit.

36. An analogue-to-digital converter comprising a multiplexer circuit according to claim 19.--

An early examination and notice of allowance are earnestly solicited.

Respectfully submitted,

DIKE, BRONSTEIN, ROBERTS & CUSHMAN LLP

Date: 9 June '00

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Case Docket No. 49,887 (301)
"Express Mail" mailing label No. EM 484715549 US
Date of Deposit June 9, 2000
I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Commissioner of Patents and Trademarks, Washington, DC 20231.

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MULTIPLEXER CIRCUIT AND ANALOGUE-TO-DIGITAL CONVERTER

The invention relates to a multiplexer circuit according to the preamble of claim 1 and to an analogue-to-digital converter (ADC) comprising such a multiplexer circuit.

In monolithic IC's transmission gates can be used for multiplexer circuits. They are suitable to select one of several analogue input channels to connect the selected channel, for example, to an ADC circuit on chip. Multiplexer circuits built with transmission gates implemented in monolithic IC's with MOS (metal oxide semiconductor) type circuits are known from CMOS Digital Integrated Circuits, Analysis and Design, S.M. Kang, Y. Leblebici, McGRAW-HILL INTERNATIONAL EDITIONS, ISBN 0-07-038046-5, page 274 and from Principles of CMOS VLSI Design, A System Perspective, second edition ADDISON WESLEY, N.H.E., Weste, K. Eshraghian, ISBN 0-201-53376-6, pages 17, 304.

An example of a conventional multiplexer circuit 1 comprising transmission gates is shown in Fig. 5. The multiplexer circuit 1 comprises at least two input channels IN_0, IN_1 which are connected with a common output channel 2. Of course, a plurality of input channels IN_0, IN_1, IN_2,... IN_i may be provided in the multiplexer circuit. For selecting one of said analogue input channels IN_0, IN_1 the multiplexer circuit comprises transmission gates FT_0, FT_1 between the input channel IN_0, IN_1 and the output channel 2, respectively. The

multiplexer can select one of the two input channels IN_0, IN_1 by select signals $SELECT_0$, $\overline{SELECT_0}$, $SELECT_1$, $\overline{SELECT_1}$ generated by a decoder circuit 10. The decoder circuit generates a select signal $SELECT_0$, $SELECT_1$ and an inverted select signal $\overline{SELECT_0}$, $\overline{SELECT_1}$ for each input channel IN_0, IN_1, respectively, which are applied to the corresponding transmission gates FT_0, FT_1. The decoder circuit is a n to 2^n decoder ($i = 2^n$), which ensures that only one of the select signals $SELECT_0$ to $SELECT_i$ becomes true while the others are false, i.e. only one channel is open while the others are closed. In the example according to Fig. 4 the channel IN_1 is selected i. e. the transmission gate FT_1 is open, whereas the channel IN_0 is not selected and the transmission gate FT_0 is closed. Analog voltages U_1, U_2 are applied to the input channels IN_0, IN_1, respectively. The voltage at the output channel 2 is indicated as U_{out}. The transmission gates FT_0, FT_1 are known CMOS transmission gates comprising p channel and n channel transistors having threshold voltages V_{THp} and V_{THn}, respectively. The multiplexer circuit is operated with a power supply voltage V_{CC} and V_{SS} is the ground potential 0V.

The operation of the multiplexer circuit is as follows. In a normal operation condition the following input voltage conditions are applied:

$$U_1 = [V_{SS}; V_{CC}]$$
$$U_2 = [V_{SS}; V_{CC}].$$

That means the level of the input voltages U_1, U_2 is between the power supply voltage level V_{CC} and V_{SS}.

Under these conditions the transmission gates FT_0 and FT_1 operate as ideal switches. Since the transmission gate FT_0 is closed, the voltage U_{out} is equal to U_2:

$$U_{out} = U_2.$$

No current will flow in the multiplexer circuit, i.e. the current in the channels IN_0 and IN_1 is 0, respectively:

$$I_{in1} = 0$$
$$I_{out} = 0.$$

In case of an over or an under voltage applied to an input channel which is not selected i. e. which is not active a current will flow through the active channel. This is the under/over voltage operation condition. The following input voltage conditions are considered as under and over voltage conditions:

Under voltage:

$$-V_{THn} + V_{SS} \leq U_1 \leq V_{SS}.$$

Over voltage:

$$V_{CC} \leq U_1 \leq V_{CC} + |V_{THp}|,$$

The voltage U_2 is:

$$U_2 = [V_{SS}; V_{CC}].$$

Under these conditions the transmission gate FT_0 in channel IN_0 does not work as an ideal switch any more. Due to "weak inversion" and the pn-diode structures of the CMOS transistors a current flows between IN_0 and IN_1.

$$\begin{matrix} |I_{in}| \geq 0 \\ |I_{out}| \geq 0 \end{matrix}$$

I_{out} creates a voltage drop at the resistance of the transmission gate FT_1 in channel IN_1 and the output resistance of the source of U_2. Therefore, U_{out} is not equal to the input voltage U_2 any more. Depending on the desired accuracy of the analogue signal this will be a problem.

In particular for multiplexer circuits used in ADC's a noise at the injection source leads to worse accuracy, which makes the conversion results unusable (e.g. in case of an 8-bit ADC the absolute accuracy becomes 10-11 LSB instead of +/-2 LSB). External over/undervoltage protection circuits are required in order to be able to use such ADC's.

It is an object of the invention to provide a multiplexer circuit and an analogue-to-digital converter having an improved accuracy with respect to the output of an analogue input signal.

The object is solved by a multiplexer circuit according to claim 1 and by an analogue-to-digital converter according to claim 12. Further developments of the invention are described in the dependent claims.

Embodiments of the invention will be explained with reference to the accompanying drawings.

Fig. 1 shows a multiplexer circuit according to a first embodiment of the invention.

Fig. 2 shows a multiplexer circuit according to a second embodiment of the invention.

Fig. 3 shows a multiplexer circuit according to the second embodiment of the invention more in detail.

Fig. 4 shows a multiplexer circuit according to a further embodiment of the multiplexer circuit of Fig. 2.

Fig. 5 shows an example of a conventional multiplexer circuit.

A first embodiment of the multiplexer circuit according to the invention is shown in Fig. 1. Parts which are the same as in the conventional multiplexer circuit according to Fig. 4 are

designated with the same reference signs and the description thereof will not be repeated.

The multiplexer circuit according to this embodiment comprises a first transmission gate FT_0, FT_1, for each channel respectively, and a second transmission gate ST_0, ST_1 for each channel. The output of the first transmission gate FT_0, FT_1 in each channel is connected with the input of the second transmission gates ST_0, ST_1, respectively. The output of the second transmission gate ST_0 and ST_1 is connected with the output channel 2. The second transmission gate ST_0, ST_1 are controlled by the same select signals $SELECT_0$, $\overline{SELECT_0}$ and $SELECT_1$, $\overline{SELECT_1}$ as the first transmission gates FT_0, FT_1.

A bypass circuit in form of an NMOS transistor 20, 21 is provided for each analogue input channel IN_0, IN_1. Each NMOS transistor 20, 21 is connected with its drain to a node 30 31. Each node 30, 31 is connected with the output of the first transmission gate FT_0, FT_1 and the input of the second transmission gate ST_0, ST_1, respectively. The source of each NMOS transistor 20, 21 is connected with the ground potential level V_{SS}. The gate of each NMOS transistor receives the inverted select signal $\overline{SELECT_0}$, $\overline{SELECT_1}$, respectively, which is generated by the channel decoder 10. In this embodiment the NMOS transistors are controlled by the same select signal as the PMOS transistor of the transmission gates.

In the example according to Fig. 1 the channel IN_1 is selected and the first transmission gate FT_1 and the second transmission gate ST_1 are both open. Since the NMOS transistor 21 receives the inverted select signal $\overline{SELECT_1}$ on its gate, the NMOS transistor 21 is switched off for the selected channel IN_1. The channel IN_0 is not selected and therefore, the first transmission gate FT_0 and the second transmission gate ST_0 are both closed. Since the NMOS transistor 20 receives the inver-

ted select signal $\overline{SELECT_0}$ on its gate, the NMOS transistor 20 is switched on for the not selected channel IN_0.

In operation the select signals are applied to the transmission gates such that the input channel IN_1 is selected by opening the first transmission gate FT_1 and the second transmission gate ST_1 by the select signal $SELECT_1$ ($SELECT_1 = 1$). The other input channel IN_0 is not selected by closing the first transmission gate FT_0 and the second transmission gate ST_0 by applying the select signal $SELECT_0$ ($SELECT_0 = 0$).

In case the voltage U_1 applied to the first input channel IN_0 has an over voltage i.e.

$$V_{CC} \leq U_1 \leq V_{CC} + |V_{THp}|,$$

a current I_{in1} flows through the first transmission gate FT_0 to node 30. Since the NMOS transistor 20 is switched on by the select signal $\overline{SELECT_0}$, the current I_{in1} is bypassed through the NMOS transistor 20 to ground. The potential at node 30 is (due to being pulled down by NMOS transistor 20) in the range of $[0, V_{CC}]$. Therefore, the transmission gate ST_0 operates as an ideal switch, i.e. closes perfectly. Therefore, the selected input channel IN_1 is not influenced by the over voltage on the first input channel IN_0. The output voltage U_{out} is equal to U_2.

Without changing the circuit in Fig. 1 the NMOS transistor 20 pulls an undervoltage $-V_{TH,N} < U_1 < 0$ at the input to a potential in the range of $[-V_{TH,N}, 0]$ at node 30. This is enough to switch the transmission gate ST_1 off and to avoid influence to the analogue input. Hence, the NMOS transistor is a measure against under voltage. However, the bypass behaviour of the NMOS transistor for over voltage condition is better than for under voltage condition.

Fig. 2 shows an embodiment of a multiplexer circuit in order to bypass the current for over or under voltage conditions. In

the embodiment according to Fig. 2 parts which are equal to parts of the embodiment according to Fig. 1 are described with the same reference signs. The multiplexer circuit according to Fig. 2 comprises a pull-down bypass circuit 50, 51 in each channel IN_0, IN_1 and in addition a pull-up bypass circuit 60, 61. The pull-down bypass circuit 50, 51 is connected between a node 70, 71 and V_{SS} level and the pull-up bypass circuit 60, 61 is connected between the node 70, 71 and V_{CC} level, respectively.

The multiplexer circuit according to Fig. 2 also comprises two operation conditions: In the normal operation condition the following input voltage conditions are applied:

$$U_1 = [V_{SS}; V_{CC}]$$
$$U_2 = [V_{SS}; V_{CC}].$$

Under these conditions the transmission gates operate as ideal switches. The voltage U_{out} is equal to U_2. No current will flow:

$$I_{in1} = 0$$
$$I_{out} = 0.$$

In an under/over voltage operation condition the following input voltage conditions are considered as under and over voltage conditions:

Under voltage:

$$-V_{THn} + V_{SS} \leq U_1 \leq V_{SS}$$

Over voltage:

$$V_{CC} \leq U_1 \leq V_{CC} + |V_{THp}|$$

(V_{THn}, V_{THp} are threshold voltages of p- and n channel transistors)

The voltage U_2 is:

$$U_2 = [V_{SS};\ V_{CC}].$$

Under these conditions the first transmission gate FT_0 in channel IN_0 does not work as an ideal switch. The current I_{in1} is bypassed to V_{SS} level or V_{CC} level by using the bypass circuit 50 or 60. The second transmission gate ST_0 is implemented in order not to change the U_{out} voltage. In case of an over/under voltage condition the bypass circuit 50 reduces the input voltage for the second transmission gate ST_0, so that no over voltage condition occurs at the second transmission gate ST_0 and the bypass circuit 60 increases the input voltage for the second transmission gate, so that no under voltage condition occurs at the second transmission gate ST_0. Therefore, the second transmission gate will work again as an ideal switch. As a result no current flows between IN_0 and IN_1 and the voltage U_{out} is equal to the input voltage U_2, i.e.

$$\begin{aligned} |I_{in1}| &\geq 0 \\ |I_{in2}| &= 0 \\ |I_{out}| &= 0 \\ U_{out} &= U_2. \end{aligned}$$

An additional circuit senses either the voltage in front of FT_0 or between FT_0 and ST_0 and switches on either the bypass circuit to V_{CC} in case of under voltage or the bypass circuit to V_{SS} in case of over voltage. This is necessary to avoid a shortcut between V_{CC} and V_{SS} via the two bypass circuits. The combination of the bypass circuit and the sense circuit forms a bypass and sense circuit.

In a further development the bypass and sense circuit contains elements to control the potential between FT_0 and ST_0.

Fig. 3 shows a specific embodiment of the multiplexer circuit according to Fig. 2. For each channel the pull-down bypass circuit 50 is realized with an NMOS transistor 80, 81 and the pull-up bypass circuit is realized with a PMOS transistor 90, 91, respectively. The NMOS transistor will be used as over voltage protection and the PMOS transistor will be used as under voltage protection on channels that are not selected.

A control circuit for the bypass circuits comprises NOR gates 100, 101, the output of which is connected with the gate of the NMOS transistor 80, 81, respectively. The control circuit further comprises NAND gates 110, 111, the output of which is connected with the gate of the PMOS transistor 90, 91, respectively. One input of the NOR gate 100, 101 is connected with the input voltage U_1, U_2, respectively, and the other input of the NOR gate 100, 101 is connected with the select signal $SELECT_0$, $SELECT_1$. One input of the NAND gate 110, 111 is connected with the input voltage U_1, U_2, respectively., and the other input of the NAND gate 110, 111 is connected with the inverted select signal $\overline{SELECT_0}$, $\overline{SELECT_1}$. Therefore, the input signals of the control circuit are the input voltage U_1, U_2 and the select and the inverted select signals which control the transmission gates. If a channel is not selected (SELECT = 0) and an under voltage condition occurs ($U_1 < 0$ V) the PMOS transistor 90 will be switched on. If a channel is not selected (SELECT = 0) and an over voltage condition occurs ($U_1 > 5$ V), the NMOS transistor 80 will be switched on.

Fig. 4 shows a second specific embodiment of the multiplexer circuit according to Fig. 2. A control circuit for controlling the bypass circuit comprises a sense circuit for sensing a voltage in the input channel. The sense circuit and the bypass circuit in combination form a bypass and sense circuit consisting of a sense path and a bypass path. In the bypass and sense circuit to V_{SS} the sense path comprises a PMOS transistor 130, 131 in series with an NMOS transistor 120, 121. The source of the PMOS transistor 130, 131 is connected

to said first transmission gate FT_0, FT_1 and the source of the NMOS transistor 120, 121 is connected to ground level V_{SS}. The drain of the PMOS transistor 130, 131 is connected with the drain of the NMOS transistor 120, 121. The bypass path is formed of NMOS transistor 160, 161 the drain of which is connected with the output of said first transmission gate FT_0, FT_1 and the source of which is connected with V_{SS} . The gate of NMOS transistor 160, 161 is connected with the drains of the PMOS and NMOS transistors of the sense circuit. The driveability of NMOS transistor 120, 121 is very weak compared to the driveability of PMOS transistor 130, 131. For a channel that is switched off a voltage of $0.65V_{DD}$ is applied to gate of PMOS 130, 131. Both the sense path and the bypass path are switched off as long as the potential at node 70, 71 fulfils the condition $U70<0.65V_{DD}+|V_{THp}|$. When due to an over voltage at the input the voltage at node 70, 71 exceeds $U70>0.65V_{DD}+|V_{THp}|$ the sense path drives a small current to V_{SS}. Because of the big impedance of NMOS 120, 121 compared to the impedance of PMOS 130, 131 the gate voltage at the gate of bypass transistor NMOS 160, 161 increases very quickly so that this transistor changes very quickly to the conducting state. In this way a low impedance path to V_{SS} is installed when the voltage U70 is close to V_{DD}. The bypass and sense circuit to V_{SS} can be associated with an ideal switch that switches on as soon as U70 approximates V_{DD}.

The pull-up bypass and sense circuit consists of NMOS 140, 141 and PMOS 150, 151 as sense path and PMOS 170, 171 as bypass path. In the bypass path, the drain of PMOS transistor 170, 171 is connected with the output 70, 71 of said first transmission gate FT_0, FT_1 and the source is connected with power supply voltage level V_{CC}. In the sense path the source of the PMOS transistor 150, 151 is connected to power supply voltage level V_{CC} and the source of the NMOS transistor 140, 141 is connected to an output 70, 71 of said first transmission gate FT_0, FT_1 and the drains of the PMOS transistor 150, 151 and the NMOS transistor 140, 141 are

connected to each other. The gate of the PMOS transistor 170, 171 is connected with the drains of the PMOS and NMOS transistors of the sense path. The bypass and sense circuit works in an analogue way for undervoltage.

Measurements on real chips prove that a subthreshold current via closed FT_0 can occur also for valid input voltages $V_{SS}<U1<V_{DD}$ dependent on the voltage drop between drain and source of FT_0. If this voltage drop is significant leakage is likely to occur due to the fact that the V_{DD} level in the chip (and at the gate of FT_0) is a little bit less than the V_{DD} level applied from externally and due to the big width of FT_0, which is necessary to achieve a small impedance if the input is active ADC input channel. The proposed bypass and sense circuits keep the voltage drop on FT_0 as small as possible and thus limit the subthreshold current into the pad. The reason is that both bypass and sense circuits are switched off for potentials U70 in the range $0.35V_{DD}-V_{THn}<U70<0.65V_{DD}+|V_{THp}|$, i.e. currents via FT_0 can only flow if one of the conditions $U70>0.65V_{DD}+|V_{THp}|$ or $U70<0.35V_{DD}-V_{THn}$ is fulfilled.

A small pad input leakage current is an important quality criteria for the IO circuit of an integrated circuit.

Of course, each of the embodiments according to Figs. 1 to 4 may comprise not only two but a plurality of input channels and each channel may have the pull-up and/or pull-down circuits and the second transmission gates as described above.

An ADC circuit according to the invention comprises a multiplexer circuit according to the embodiments of Figs. 1 to 4 where the output voltage U_{OUT} of the multiplexer is the input voltage for the ADC. The accuracy of such an ADC can be as good as without over/undervoltage, i.e. the over/undervoltage has no influence to the conversion result (e.g. in case of an 8-bit ADC the accuracy is +/-2 LSB with or without over/undervoltage).

C L A I M S

1. Multiplexer circuit
comprising at least two input channels (IN_0, IN_1) and an output channel (2),
each input channel (IN_0, IN_1) comprising a first transmission gate (FT_0, FT_1) which can be switched on by a select signal ($SELECT_0$, $\overline{SELECT_0}$; $SELECT_1$, $\overline{SELECT_1}$) for connecting the input channel (IN_0, IN_1) to the output channel (2),
at least one of the input channels (IN_0, IN_1) comprising a bypass circuit (20, 21; 50, 51; 60, 61; 80, 81; 90, 91; 160, 161; 170, 171) for preventing a current flowing through the first transmission gate (FT_0, FT_1) from reaching the other input channel,
and a second transmission gate (ST_0, ST_1), characterized in that a control circuit is provided for controlling said bypass circuit.

2. Multiplexer circuit according to claim 1, wherein said control circuit controls said bypass circuit dependent upon a voltage in the input channel (IN_0; IN_1).

3. Multiplexer circuit according to claim 1, or 2,
wherein said control circuit comprises a sense circuit (120, 130; 121, 131; 140, 150; 141, 151; 100, 110; 101, 111) to control said bypass circuit (80, 90; 81, 91; 160, 161; 170, 171) by sensing a voltage in the input channel (IN_0; IN_1).

4. Multiplexer circuit according to one of claims 1 to 3,
wherein each input channel (IN_0, IN_1) comprises a bypass circuit (20, 21; 50, 51; 60, 61; 80, 81; 90, 91; 160, 161; 170, 171) and a second transmission gate (ST_0, ST_1).

5. Multiplexer circuit according to claim 4, wherein the bypass circuit (20, 21; 50, 51; 60, 61) is switched on for an

input channel (IN_0) which is not selected and is switched off for a selected input channel (IN_1).

6. Multiplexer circuit according to one of claims 1 to 5, wherein said bypass circuit comprises a pull-down circuit (20, 21; 50, 51; 80, 81; 160, 161) reducing an input voltage for the second transmission gate (ST_0, ST_1).

7. Multiplexer circuit according to one of claims 1 to 6, wherein said bypass circuit (20, 21) is controlled by said select signal ($\overline{SELECT_0}$, $\overline{SELECT_1}$).

8. Multiplexer circuit according to one of claims 1 to 7, wherein said bypass circuit (20, 21; 50, 51) is an NMOS transistor the gate of which is controlled by said select signal ($\overline{SELECT_0}$, $\overline{SELECT_1}$), the drain of which is connected with an output of said first transmission gate (FT_0, FT_1) and the source of which is connected with ground potential (V_{SS}).

9. Multiplexer circuit according to one of claims 1 to 8, wherein said bypass circuit comprises a pull-up circuit (60, 61; 90, 91; 170, 171) increasing an input voltage for said second transmission gate (ST_0, ST_1).

10. Multiplexer circuit according to claim 9, wherein said pull-up circuit (60, 61; 90, 91; 170, 171) is a PMOS transistor the drain of which is connected with an output of said first transmission gate (FT_0, FT_1) and the source of which is connected with a power supply voltage level (V_{CC}).

11. Multiplexer circuit according to claims 1 to 10, wherein said control circuit controls said bypass circuit by means of said select signal ($SELECT_0$, $\overline{SELECT_0}$; $SELECT_1$, $\overline{SELECT_1}$) and an input voltage (U_1, U_2) applied to said input channel (IN_0, IN_1).

12. Multiplexer circuit according to claims 8 to 11, wherein said control circuit controls said pull-up circuit (60, 61) and said pull-down circuit (50, 51) by means of said select signal ($SELECT_0$, $\overline{SELECT_0}$; $SELECT_1$, $\overline{SELECT_1}$) and an input voltage (U_1, U_2) applied to said input channel (IN_0, IN_1).

13. Multiplexer circuit according to claim 12, wherein said control circuit comprises a NAND gate (110, 111) the output of which is connected with the gate of said PMOS transistor (90, 91) and a NOR gate (100, 101) the output of which is connected with the gate of said NMOS transistor (80, 81).

14. Multiplexer circuit according to claim 13, wherein said NAND gate receives the input voltage and the inverted select signal ($\overline{SELECT_0}$, $\overline{SELECT_1}$) and said NOR gate receives the input voltage and the select signal ($SELECT_0$, $SELECT_1$).

15. Multiplexer circuit according to one of claims 2 to 10, wherein said sense circuit (120, 130; 121, 131; 140, 150; 141 151) is formed so as to sense a voltage in the input channel (IN_0, IN_1) at the input of said first transmission gate (FT_0, FT_1)or between said first transmission gate (FT_0, FT_1) and said second transmission gate (ST_0, ST_1).

16. Multiplexer circuit according to claim 15, wherein a pull-down bypass circuit is formed of a NMOS transistor (160; 161) the drain of which is connected with an output (70, 71) of said first transmission gate (FT_0, FT_1) and the source of which is connected with the ground level (V_{SS}) and wherein said sense circuit is formed of a PMOS transistor (130; 131) and an NMOS transistor (120; 121) in series the source of the NMOS transistor (120; 121) being connected to ground level (V_{SS}) and the source of PMOS transistor (130; 131) being connected to an output (70, 71) of said first transmission gate (FT0, FT1) and wherein the drains of said PMOS transistor (130; 131) and said NMOS transistor (120; 121) are connected

to each other and to the gate of the NMOS bypass transistor (160; 161).

17. Multiplexer circuit according to claim 15 or 16, wherein said pull up bypass circuit is formed of a PMOS transistor (170; 171) the drain of which is connected with an output (70; 71) of said first transmission gate (FT_0, FT_1) and the source of which is connected with power supply voltage level (V_{CC}) and wherein said sense circuit is formed of a PMOS transistor (150; 151) and an NMOS transistor (140; 141) in series the source of the PMOS transistor (150; 151) being connected to power supply voltage level (V_{CC}) and the source of the NMOS transistor (140; 141) being connected to an output (70; 71) of said first transmission gate (FT_0, FT_1) and wherein the drains of the PMOS transistor (150; 151) and the NMOS transistor (140; 141) are connected to each other and to the gate of the PMOS bypass transistor (170, 171).

18. Analogue-to-digital converter comprising a multiplexer circuit according to one of claims 1 to 17.

ABSTRACT

A multiplexer circuit (100) comprises at least two input channels (IN_0, IN_1) and an output channel (2), each input channel (IN_0, IN_1) comprising a first transmission gate (FT_0, FT_1) which can be switched by a select signal ($SELECT_0$, $\overline{SELECT_0}$; $SELECT_1$, $\overline{SELECT_1}$) for connecting the input channel (IN_0, IN_1) to the output channel (2), and wherein at least one of the input channels (IN_0, IN_1) comprises a bypass circuit for preventing a current flowing through the first transmission gate (FT_0, FT_1) from reaching the other input channel, and a second transmission gate (ST_0, ST_1).

(Fig. 2)

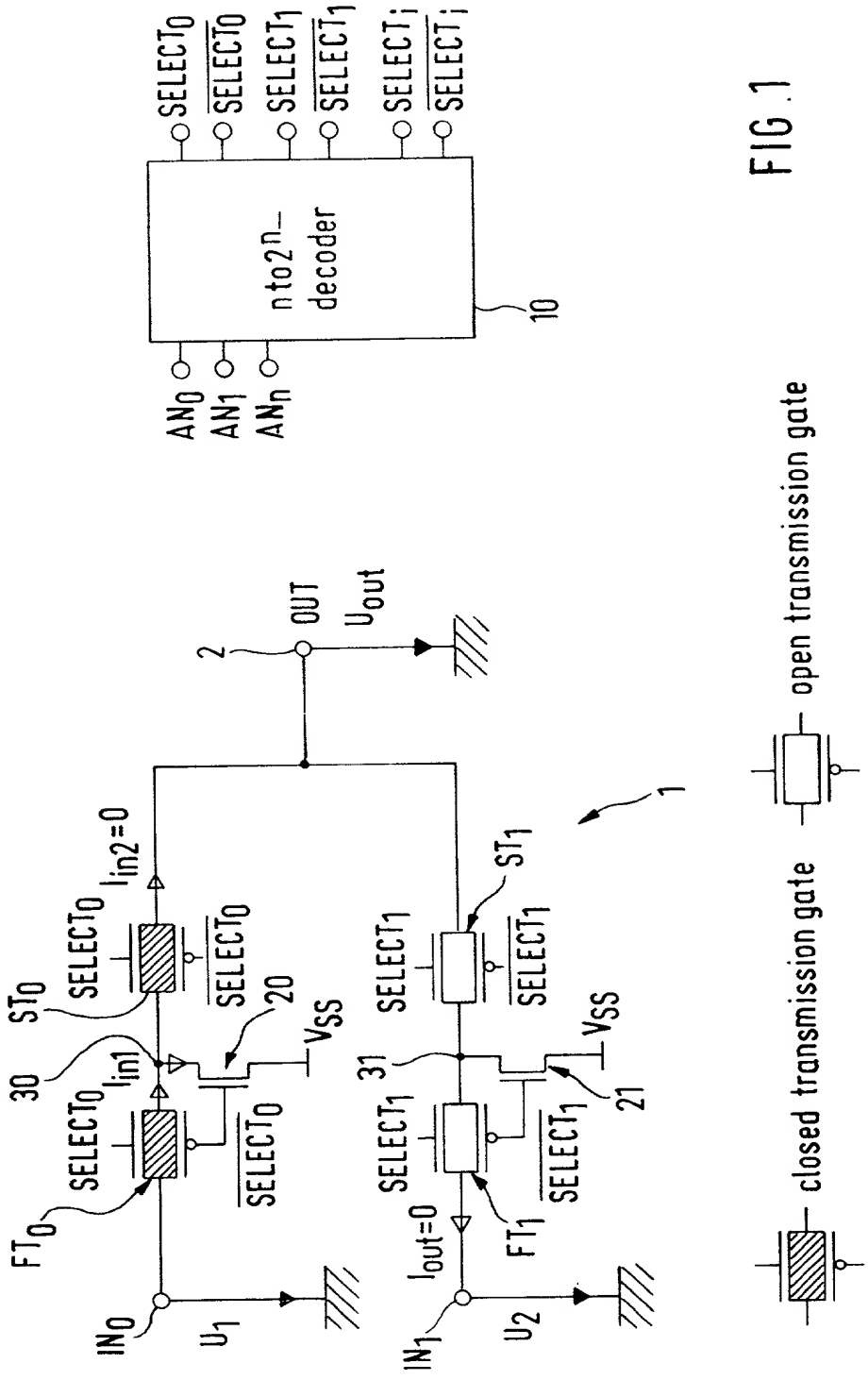

SELECT0
SELECT0
SELECT1
SELECT1
SELECTi
SELECTi
n to 2^n- decoder
10
AN0
AN1
ANn
2
OUT
Uout
1
ST1
SELECT1
SELECT1
Vss
31
21
SELECT1
SELECT1
FT1
Iout=0
IN1
U2
Iin2=0
ST0
SELECT0
SELECT0
20
Vss
30
Iin1
SELECT0
SELECT0
FT0
IN0
U1
closed transmission gate
open transmission gate

FIG 1

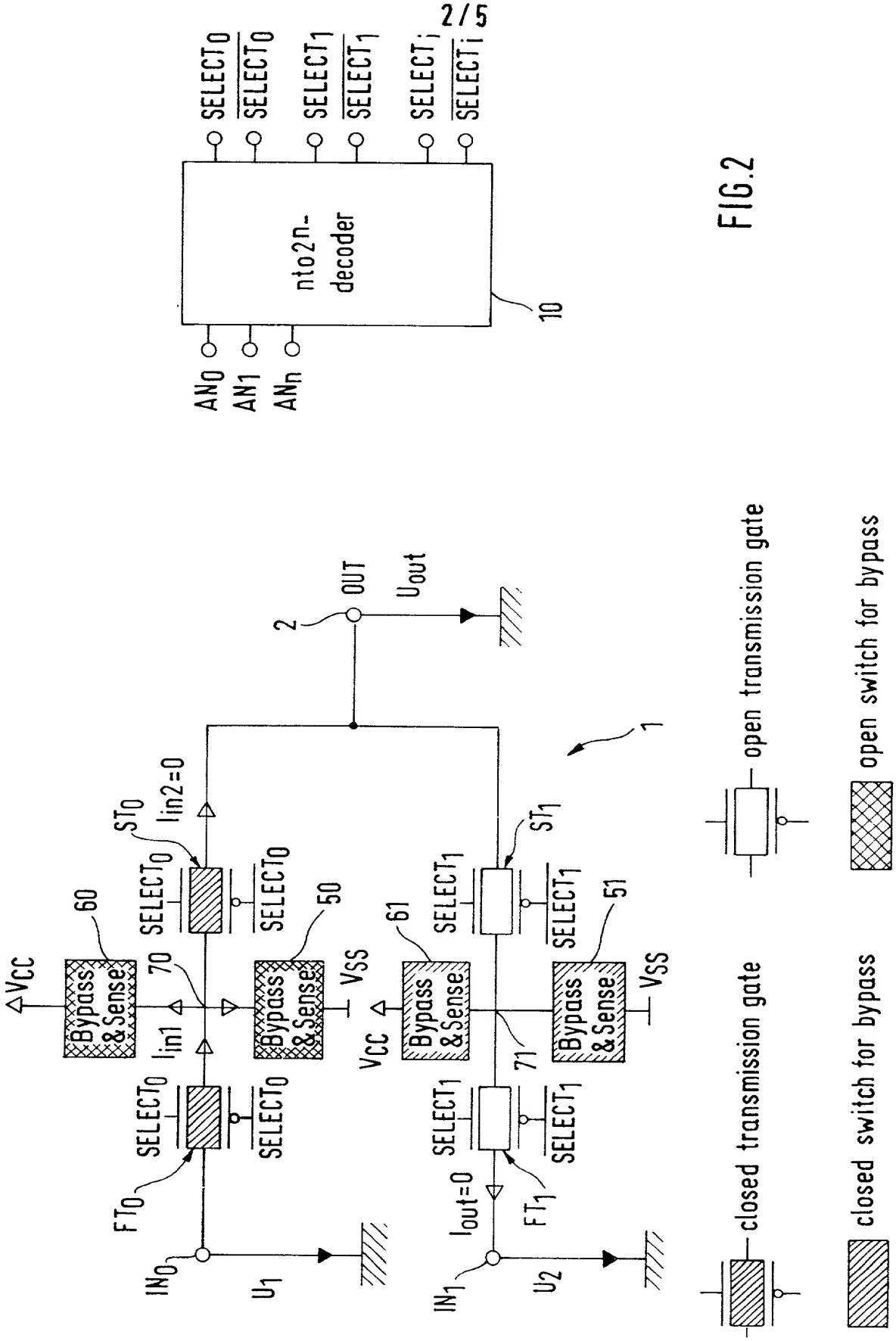
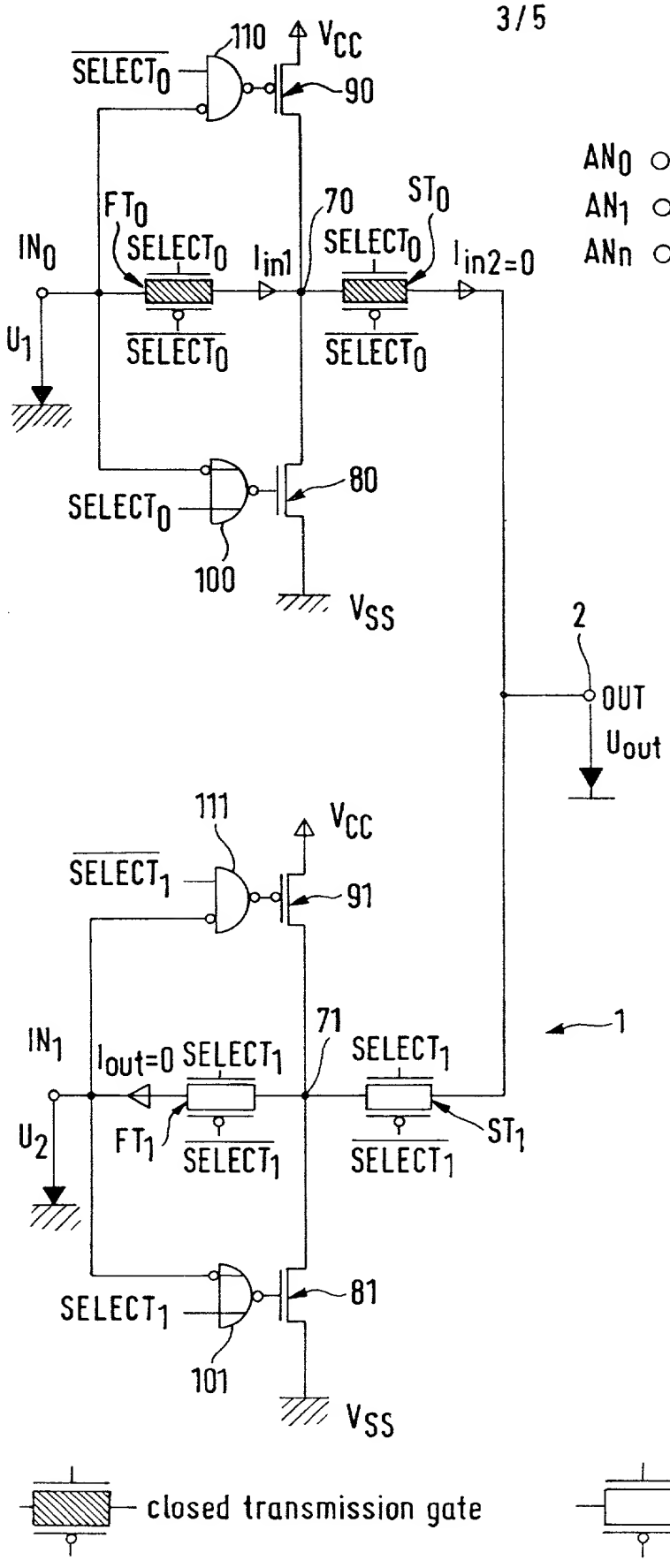
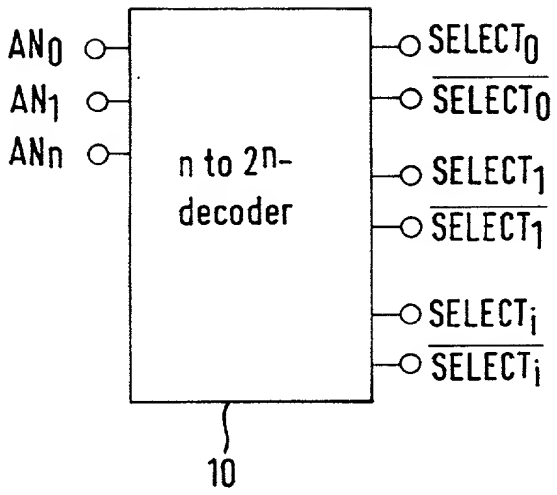

SELECT0
SELECT0
SELECT1
SELECT1
SELECTi
SELECTi
nto2n-
decoder
10
AN0
AN1
ANn
OUT
Uout
2
1
Vcc
Bypass
&Sense
60
70
50
61
51
71
Vss
ST0
Iin2=0
Iin1
FT0
IN0
U1
Iout=0
FT1
IN1
U2
ST1
open transmission gate
closed transmission gate
open switch for bypass
closed switch for bypass

FIG.2

FIG.3


110
V_{CC}
$\overline{SELECT_0}$
90
FT_0
70
ST_0
IN_0
$SELECT_0$
I_{in1}
$SELECT_0$
$I_{in2=0}$
U_1
$\overline{SELECT_0}$
$\overline{SELECT_0}$
80
$SELECT_0$
100
V_{SS}
2
OUT
U_{out}
111
V_{CC}
$\overline{SELECT_1}$
91
71
1
IN_1
$I_{out=0}$
$SELECT_1$
$SELECT_1$
U_2
FT_1
ST_1
$\overline{SELECT_1}$
$\overline{SELECT_1}$
$SELECT_1$
81
101
V_{SS}


AN_0
AN_1
ANn
n to 2^n-decoder
$SELECT_0$
$\overline{SELECT_0}$
$SELECT_1$
$\overline{SELECT_1}$
$SELECT_i$
$\overline{SELECT_i}$
10

closed transmission gate

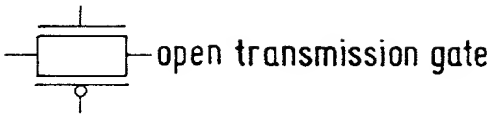
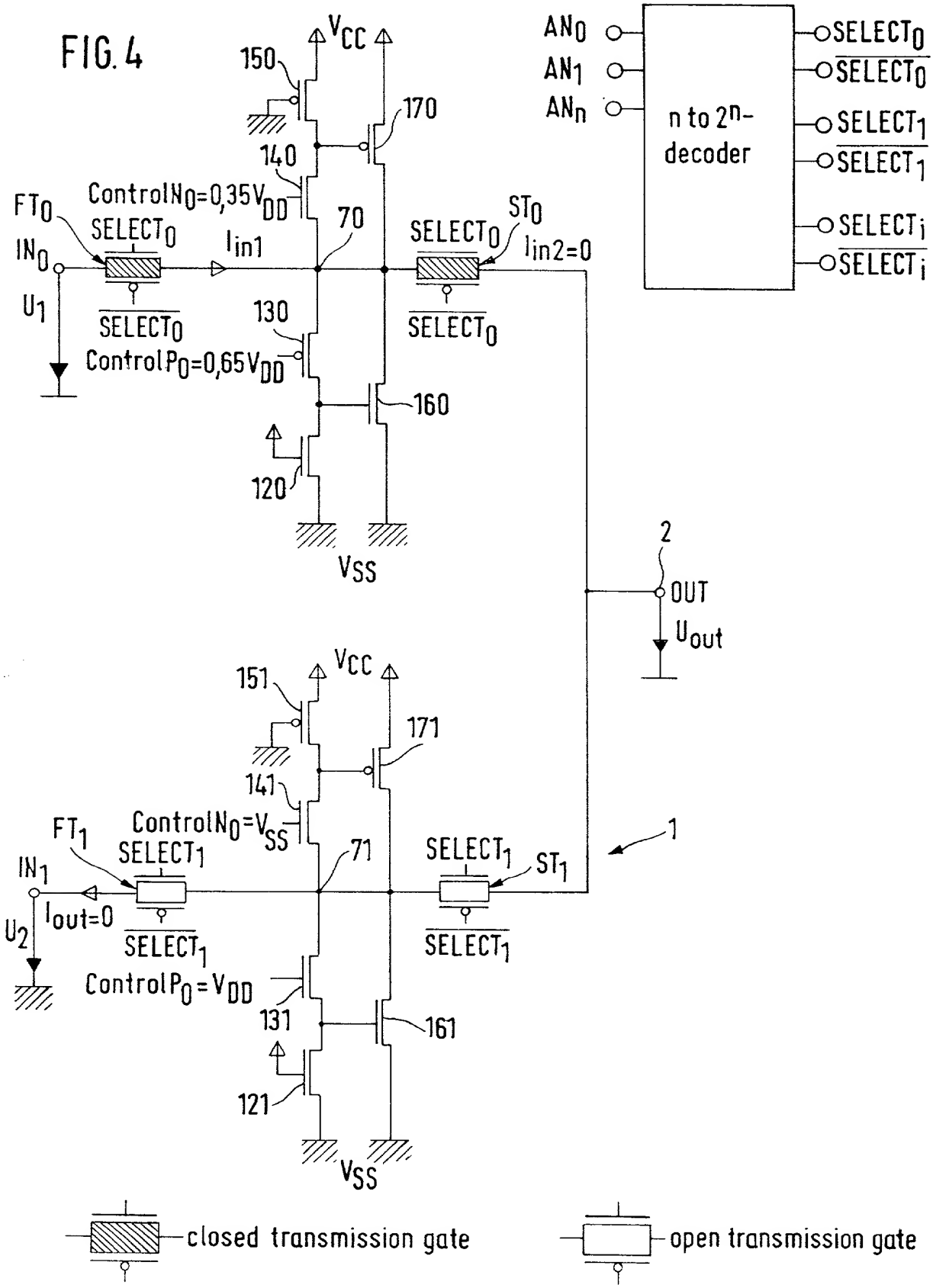

open transmission gate

FIG. 4


AN0
AN1
ANn
n to 2n-decoder
SELECT0
SELECT0
SELECT1
SELECT1
SELECTi
SELECTi
VCC
150
170
140
ControlN0=0,35VDD
FT0
SELECT0
IN0
Iin1
70
ST0
SELECT0
Iin2=0
U1
SELECT0
SELECT0
130
ControlP0=0,65VDD
160
120
VSS
2
OUT
Uout
151
VCC
171
141
ControlN0=VSS
FT1
SELECT1
71
SELECT1
ST1
1
IN1
Iout=0
U2
SELECT1
SELECT1
ControlP0=VDD
131
161
121
VSS
closed transmission gate
open transmission gate

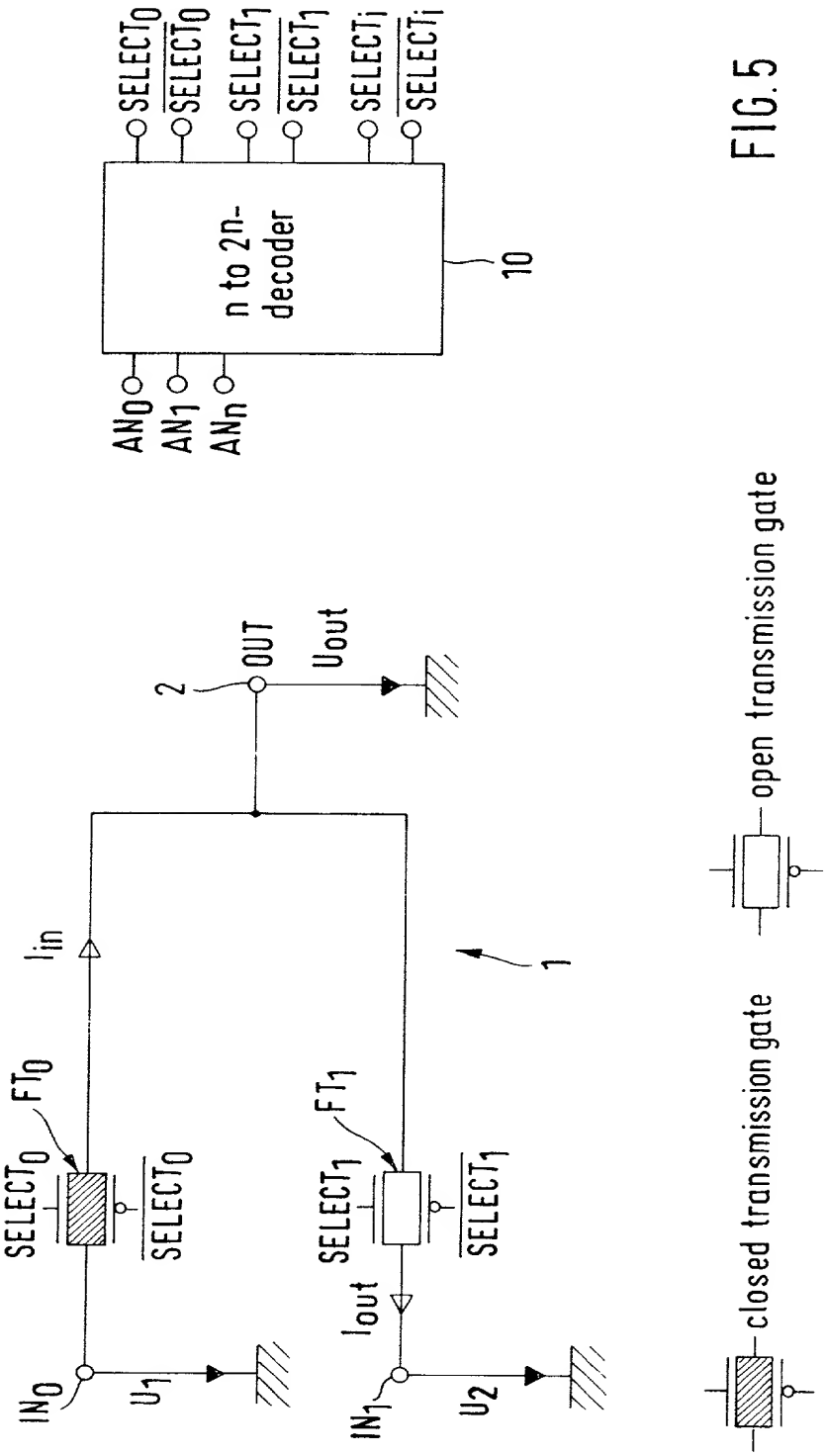

SELECT0
SELECT0
SELECT1
SELECT1
SELECTi
SELECTi
n to 2n-decoder
10
AN0
AN1
ANn
2
OUT
Uout
Iin
FT0
SELECT0
SELECT0
FT1
SELECT1
SELECT1
1
Iout
IN0
U1
IN1
U2
open transmission gate
closed transmission gate

FIG.5

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Docket No. 49887 (301)

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that: My residence, post office address and citizenship are as stated below next to my name. I believe I am the original, first and sole inventor (if only one name is listed at 201) below or an original, first and joint inventor (if plural names are listed at 201-206 below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: **MULTIPLEXER CIRCUIT AND ANALOGUE-TO-DIGITAL CONVERTER**

which is described and claimed in:

☐ the specification attached hereto.

☒ the specification in U.S. Application Serial Number 09/581,464, filed on June 9, 2000.

☐ the specification in PCT international application Number, filed on _____; and was amended on _____.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a). I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed

Prior Foreign/PCT Applications and Any Priority Claims Under 35 U.S.C. §119:			
Application No.	**Filing Date**	**Country**	**Priority Claimed Under 35 U.S.C. §119?**
98 119 148.9	September 10, 1998	Europe	XXX☐YES ☐NO
PCT/EP99/07531	July 10, 1999	PCT	XX☒YES ☐NO
			☐YES ☐NO

I hereby claim the benefit under 35 U.S.C. §120 of any United States application(s) or PCT international application(s) designating the United States of America that is/are listed below, and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of 35 U.S.C. §112, I acknowledge the duty to disclose material information as defined in 37 CFR §1.56(a) which occurred between the filing date of the prior application(s) and the national or PCT international filing date of this application:

Prior U.S. Applications or PCT International Applications Designating the U.S-Benefit Under 35 U.S.C. §120

U.S. Applications		Status (Check One)		
Application Serial No.	**U.S. Filing Date**	**Patented**	**Pending**	**Abandoned**

PCT Applications Designating the U.S.					
Application No.	**Filing Date**	**U.S. Serial No. Assigned**			

CLAIM FOR BENEFIT OF PRIOR U.S. PROVISIONAL APPLICATION(S) (35 U.S.C. §119(e))

I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States provisional application(s) listed below:

Applicant	Provisional Application Number	Filing Date

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) with full powers of association, substitution and revocation to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

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	POST OFFICE ADDRESS	POST OFFICE ADDRESS	CITY	STATE OR COUNTRY AND ZIP CODE
205	FULL NAME OF INVENTOR	LAST NAME	FIRST NAME	MIDDLE NAME
	RESIDENCE & CITIZENSHIP	CITY	STATE OR FOREIGN COUNTRY	COUNTRY OF CITIZENSHIP
	POST OFFICE ADDRESS	POST OFFICE ADDRESS	CITY	STATE OR COUNTRY AND ZIP CODE
206	FULL NAME OF INVENTOR	LAST NAME	FIRST NAME	MIDDLE NAME
	RESIDENCE & CITIZENSHIP	CITY	STATE OR FOREIGN COUNTRY	COUNTRY OF CITIZENSHIP
	POST OFFICE ADDRESS	POST OFFICE ADDRESS	CITY	STATE OR COUNTRY AND ZIP CODE

I hereby further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon

Signature of Inventor **201**	Signature of Inventor **202**
Date: July 26, 2000	Date: July 26, 2000
Signature of Inventor **203**	Signature of Inventor **204**
Date: July 26, 2000	Date:
Signature of Inventor **205**	Signature of Inventor **206**
Date:	Date: